Seat No.			Set P
	M.Sc. (Seme	ester - I) (CBCS) Exa Electronia NUMERICAL MI	
•	ate: Thursday, 16).30 AM to 01.00 F		Max. Marks: 70
Instruct	2) Answer a 3) Answer fi	d (2) are compulsory. Iny three questions from ive questions. o the right indicate full m	
Q.1 A	1) On Laplace t a) Time dom b) Frequenc c) Time dom	ernatives given below. transformation, the funct nain to frequency domai cy domain to time domai nain to amplitude domain e domain to time domair	า า
	2) If data consis method gene a) n th c) (n-1) th	erates the polynomial of b	en Newton's forward interpolation order.) (n+1) th) Second
	 For set of po suitable. a) Cubic spl c) Lagrangia 	lines b)	method of interpolation is Newton's forward difference All of these
	,	atrix. iangular b)	, the coefficient matrix is reduced to Identity Upper Triangular
	5) Laplace Trar a) 1/S c) (24)/S ⁵	nsform of f(t) = t ⁴ is giver b) d)	h by F(s)= (4)/(S) (6)/(S ⁴)
	of equations. a) Tridiagon	Ial b) d)	ved by using matrix system U-matrix All of these
	7) For Newtons a) E ² c) (E+1) ²	forward difference $\Delta^2 Y_0$ b) d	= (E-1) ² All of these
	8) The Least so	quares method of curve	itting is developed by considering
	,	tion of data points	arrara

- b) Minimization of sum of squares of errors
 c) Maximization of data points
 d) Maximization of errors

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	 B) State True or false. 1) Forward substitution method is adopted for U-matrix. 2) On Laplace Transformation, an expression for current response through RL circuit consists of two parts DC and transient. 3) Newton-Cotes integration formula for three points reduces to Sompson's one third rule. 4) For solving ODE by Eulers method, final value of the function is considered. 5) For cubic splines only two points are considered. 6) The matrix of single column is called vector. 	06
Q.2	A) Attempt any two.	10
	 Derive expression for Laplace transformation of f(t) = coswt What do you mean by forward and backward substitution method for solution of system of equation? Solve x₁ - x₂ + 2x₃ = 4 2x₁ + 4x₂ + x₃ = 6 x₁ + x₂ + 5x₃ = -2 	
	B) Write a note on Piece-wise linear analysis.	04
Q.3	A) Describe formation of system of linear equations? Describe Gaussian	08
	Jordon elimination method for solution of system of linear equations.	00
	B) Evaluate by using Simpson's one third rule for 10 points. $I = \int_{0}^{1} e^{-x} x$	06
Q.4	a) What do you mean by Laplace Transformation and Inverse Transformation?	08
	With suitable example describe partial fraction rule. b) Obtain Laplace Inverse Transformation of the function	06
	$F(S) = \frac{1}{(s+5)(s-3)}$	00
0.5	a) Using Newton's forward interpolation formula derives the expression for first	00
Q.5	order and second order numerical differentiation.	80
	b) Find first and second order derivative for following data $x = 6$.	06
	X 2 4 6 8 10 Y 1.583 1.797 2.044 2.325 2.651	
Q.6	a) What do you mean by quadrature? Describe in detail the Newton Cote	08
Q.0	formal for numerical integration. Obtain expression for Simpson mid-point	00
	and one third rule.	06
	b) Evaluate by using trapezoidal rule for 10 points.	06
	$I = \int_{0}^{\infty} dx / (1+x)$	
Q.7	a) Using Taylers series derive the expression for solution of ODE for RK-II	08
	order method. b) Using RK-II order method find value of y(0.2) Given that	06
	$\frac{dy}{dx} = x^2 - y \text{ and } y(0) = 1$	
	dx x y $and y (0) = 1$	

M.Sc. (Semester - I) (CBCS) Ex Electron	ics
INSTRUMENTATI Day & Date: Saturday, 18-11-2017 Time: 10.30 AM to 01.00 PM	Max. Marks: 70
Instructions: 1) Q. (1) and (2) are compulsory. 2) Answer any three questions from 3) Answer any 5 questions. 4) Figures to the right indicates full	
c) Distance between two plates2) Which of the following has proper distance	acitance is depends upon b) Effective area of the plate d) All of these
 3) To measure physical parameters, in bridge would be used. a) AC c) Capacitive 4) For signal conditioning of both AC a most suitable monolithic signal condition a) IC-2B31 c) IC-2B30 	 b) DC d) All of these as well as DC signal, is the
5) In case of LVDT, when core is at nuccorrect? a) $E_{s_1} > E_{s_2}$ c) $E_{s_1} = E_{s_2}$ 6) Chromel – Alumel thermocouple is one of the second seco	b) $E_{s_1} < E_{s_2}$ d) None of the above
 7) The recorder, in which one of the vacalled a) X-T recorder c) X-Y recorder 	,
 8) The temperature coefficient of the s a) 25m V/⁰K c) 10m V/⁰K B) State True or false. 	ensor LM35 is b) 10m V/ ⁰ C d) None of these 06
 Isolation amplifier is used to isolate amplifier. Electromagnetic chielding is used for 	the stages in instrumentation

- 2) Electromagnetic shielding is used for coupling with two circuitry.
 3) For the single channel DAS the IC 0808 ADC is used because it has only one analog channel.

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		 The sensor SY-HS-220 is precision humidity sensor. If transducted signal has a range of 0m V to 100m V and reference voltage for ADC is 2.56 volt, then gain of instrumentation amplifier should be more than 100 to avoid saturation. For JK thermocouple AD595 is most suitable instrumentation amplifier. 	
Q.2	A)	 Attempt any two of the following. 1) What is need of DAS? 2) Write a note on selection criteria for transducer. 3) Explain general block diagram of measuring instrument. 	10
	B)	Explain in detail, Isolation amplifier.	04
Q.3	-	Explain construction and working principle of the thermocouple. Write a note on V-F converter.	08 06
Q.4	-	What do you mean by recorder? Explain in detail the Strip chart recorder. Write a note on 2B30 the programmable signal conditioner.	08 06
Q.5		Explain in detail the static as well as dynamic characteristics of sensors. Write a note on Multi-channel DAS.	08 06
Q.6		Explain the concept of grounding and shielding? Write a note on AD620 as instrumentation amplifier.	08 06
	•	Explain the method used to measure used to measure liquid level precisely.	06
Q.7		Explain strain gauge and derive the expression for gauge factor. What do you mean by LCD, which should be used for measurement instrumentation?	08 06

Electronics POWER ELECTRONICS Day & Date: Tuesday, 21-11-2017 Time: 10.30 AM to 01.00 PM 2) Q. (1) and (2) are compulsory. 2) Answer any three questions from Q.3 to Q.7. 3) Figures to the right indicates full marks. a) AC b) DC d) None of these c) Both a & b assumption that load current is _____ during the communication period. a) Varies b) Decreases d) Constant b) Inductors c) Both a & b d) None of these

Instructions: 1) Attempt five questions.

Q.1 A) Choose the alternatives given below.

- 1) The _____ voltage controller is used in speed control of Induction motor.
- 2) In the operation of McMurry half bridge inverter is based on the

 - c) Increases
- 3) In McMurry half-bridge inverter _____ are the commutating components.
 - a) Capacitors

 In case of step down cycloconverter the output frequency is _____ supply frequency.

- a) Less than b) Greater than
- c) Equal to d) None of these
- 5) The chopper is _____ converter.
 - a) AC to DC b) DC to AC
 - c) AC to AC d) DC to DC
- 6) In three phase half wave controlled rectifier for interval $\alpha \ge \pi/6$, the average load voltage is given by _____
 - a) $\frac{3Vm}{2\pi} \left[1 + \cos\left(\frac{\pi}{6} + \alpha\right) \right]$
 - c) $\frac{Vm}{2\pi} [\cos \alpha 1]$

b) $\frac{Vm}{2\pi} [\cos \alpha + 1]$

d) None of thee

d) All of these

b) Speed control of DC motor

- 7) The _____ is application of AC voltage controllers.
 - a) Lighting control
 - c) AC magnet control
- 8) In voltage source inverter output AC voltage depends on _____ voltage.
 - a) Input AC
 - b) Input DC c) Both a & b d) None of these

B) State True or false.

- 1) The RMS load voltage for integral cycle control is $Vs\sqrt{K}$.
- 2) The rectifier is DC to AC convertor.

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M.Sc. (Semester - I) (CBCS) Examination Oct/Nov-2017

Max. Marks: 70

08

06

		3) In phase operation of multiphase chopper, it turn on and off at a different instant.	
		4) In symmetrical configuration of single phase full wave half controlled bridge rectifier, angle for all the devices is $\pi - \alpha$ rad.	
		 5) In McMurry Bedford communication the feedback diode are equally effective in centre taped circuits catering for inductive loads. 6) In type A chopper, SCR is turned off when its current drops below its holding current value for specific duration. 	
Q.2	A)	Attempt any two. (Short Questions)	10
		1) State the advantages & disadvantage of unidirectional and bidirectional controllers.	
		2) Write a note on single phase full wave full controlled bridge rectifier with R load.	
		3) Write a note on class C chopper.	
	B)	Explain integral cycle controller.	04
Q.3		Explain three to single phase cycloconverter. Explain half controller bridge rectifier with free wheeling diode.	07 07
Q.4		Explain single phase full bridge inverter. Explain step up and step down chopper.	07 07
Q.5	a)	With neat circuit diagram and waveform explain the operation of full wave controlled rectifier with inductive load.	07
	b)	Derive the relations for average output voltage and RMS output voltage full wave controlled rectifier with inductive load.	07
Q.6		Explain with suitable waveform three phase unidirectional controller. Explain McMurry full bridge inverter.	07 07
Q.7		Explain in detail single PWM and multiphase PWM inverters. Explain in detail mid point and bridge type cycloconverter.	07 07

Seat No.			S	et	Ρ
		ter - I) (CBCS) Exam Electronics ANCED MICROCON	ination Oct/Nov-2017 TROLLERS		
	Date: Thursday, 23-1 10.30 AM to 01.00 PN		Max. M	larks:	70
Instruc	3) Answer an	 five questions. and 2 are compulsory. three questions from Q.3 e right indicates full mark 			
		,	Active High Low to High		08
	2) Each Port pin of A a) 10 c) 15	VR atmega8 Microcontro b) 2 d) 2		IA.	
	 3) PIC 16F877 micro a) 36 x8 c) 38x8 	b) 3	bytes of Data Memory (RAM) 668x8 668 x14		
	4) In AVR a) R26 – R27 c) R30 – R31	,	gister. R28 – R29 None of these		
	5) PIC microcontrolle a) Controller c) Both a & b		Set Computer None of these		
	6) is used a) R0 c) R2	,	/R Microcontroller. R1 R3		
	7) Interrupt of PIC m a) F5h to 00h c) FFh to 00h	,	overflow from F0h to 00h None of these		
	8) Resiste a) GIMSK c) ADMUX	,	le external interrupts. GMSK None of these		
	 2) PIC 16F877 has 3 3) AVR atmega8 mid 4) To select Bank 2 register is set. 5) AVR atmega8 mid 	DN1 is used for Result Fo 5 two word instructions. rocontroller has 4 resister	r banks. er at a time, the IRP bit of sta al purpose registers.		06

6) PORTB of PIC microcontroller has a weak internal pull-up.

Q.2	a)	 Answer any two of the following. 1) Write note on Addressing Modes of AVR atmega8. 2) Write note on PWM mode of PIC microcontroller. 3) Write note on resister bank of PIC 16F877 microcontroller. 	10
	b)	Compare LP and ST instructions of AVR microcontroller.	04
Q.3		Write a note on Architecture of AVR microcontroller. Explain in detail arithmetic and data transfer instructions of PIC microcontroller.	08 06
Q.4		Explain in detail interfacing of LCD to PIC microcontroller. Write a note on Timer 1 of AVR microcontroller.	08 06
Q.5		Explain compare and capture mode of PIC microcontroller. Write note on features of AVR microcontroller.	08 06
Q.6		Write a note WDT mode of PIC microcontroller. Explain firing of thyristor using PIC 16F877 microcontroller.	08 06
Q.7		What do you mean by Power on reset and Brown out reset? Write note on clock and reset circuit of AVR microcontroller.	08 06

No.					Jei
	M.Sc. (Semester	- III) (New)) (CBCS) Examination	Oct/Nov-2017

Day & Date: Thursday, 16-11-2017 Time: 02.30 PM to 05.00 PM

Seat

Instructions: 1) Attempt five questions.

- 2) Q. (1) and (2) are compulsory.
- 2) Answer any three questions from Q.3 to Q.7.
- 3) Figures to the right indicate full marks.

Q.1 A) Choose the alternatives given below.

- 1) The important characteristics of ideal filters are _____
 - a) Ideal filters have constant gain in the passband and zero gain in the stop band
 - b) Ideal filters have zero gain in the passband and constant gain in the stop band
 - c) Ideal filters has nonlinear phase response
 - d) Ideal filters have zero gain in the passband and stop band

Electronics DIGITAL SIGNAL PROCESSING

- 2) If x(n) is causal sequence then its final value is _
 - a) $x(0) = \lim_{z \to \infty} X(Z)$ b) $x(0) = \lim_{z \to 0} X(Z)$ c) $x(\infty) = \lim_{z \to 1} X(Z)$ d) $x(\infty) = \lim_{z \to 1} X(Z) (1 - Z^{-1})$
- 3) If x(n) is anticausal sequence then ROC is ______.
 - a) Interior part of circle of radius $\boldsymbol{\alpha}$
 - b) Exterior part of circle of radius $\boldsymbol{\alpha}$
 - c) Intersection of two circles of radii α & β
 - d) Entire Z plane except $|Z| = 0 \& |Z| = \infty$
- In DIT FET algorithm obtaining N-point DFT _____ numbers of multiplications are required.
 - a) N^2 b) $N^2 - N$ c) $\frac{N}{2} \log_2 N$ d) $N \log_2 N$

5) The advantages of bilinear transformation method are _____.

- a) The mapping is one to one
- b) There is no aliasing effect
- c) There is one to one transformation from the s-domain to z-domain.
- d) All of above
- 6) The DFT of delayed unit impulse $\delta(n n_0)$ is _____
 - a) $e^{-j2\pi i k n 0/N}$ b) $e^{j2\pi i k n 0/N}$
 - c) $e^{j\pi i k n \ 0/N}$ d) $e^{-j\pi i k n \ 0/N}$
- The necessary condition to use the practical low pass filter without any distortion is _____.

a) f _s < 2w	b) f _s > 2w
c) $f_s = 2w$	d) f _s > w

Max. Marks: 70

Set

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08

	 8) If x(t) is odd then X(jω) a) Imaginary & even b) Imaginary & odd c) Real & odd d) Real & even B) State True or false.	06
	 b) State True of faise. 1) Using VLSI technology, the hardware of analog filter can be reduced. 2) If the signal is shifted in frequency, the magnitude spectrum does not change but only the phase spectrum will be altered. 3) Convolution of two sequences in the time domain is equivalent to multiplication of its Z- transforms in Z domain. 4) Analog filter is stable if the poles lie on the L.H.S. of s-plane. 5) In Symmetry property of DFT, when x (n) is real valued then X(N-K)=X*(K) 6) The multiplication of any sequence with u(-n-1) gives casual sequence. 	00
Q.2	 A) Attempt any two. 1) Explain how sampling can be done with an impulse function. 2) Write short note on bilinear transformation. 3) Obtain the z-transform finite duration sequence x(n)={1,2,4,3,5,7} 	10
	B) Explain development of fourier transform.	04
Q.3	A) Given $x(n) = 2^n$ and N=8, find X(K) using DIT FFT algorithms. B) Find the 4 point DFT of given window function, $w(n) = u(n) - u(n-N)$	08 06
Q.4	A) An analog filter has the following transfer functions $H(S) = 1/(S+1)$ using	08
	 bilinear. B) Determine the Z transform and ROC of the given signal x(n) = 2ⁿ⁺²[u(n-1)]. Is the signal is causal? 	06
Q.5	 A) State and prove parseval's theorem of DFT. B) Explain bilinear transformation for IIR filter design. 	08 06
Q.6	A) Find the Fourier transform of the signal shown in figure.	08
	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	

- B) Find Fourier transform and sketch the magnitude spectrum of unit Step06 function.
- **Q.7 A)** Using graphical method, obtain a 4- point circular convolution of two DT **08** signals defined as, $x(n) = \{1,2,3,1\}$ and $h(n) = \{4,3,2,2\}$
 - **B)** Use residue method to obtain x(n) from $X(Z) = Z(Z+1)/(Z-1)^2$ 06

No.	Set P
	M.Sc. (Semester - III) (New) (CBCS) Examination Oct/Nov-2017 Electronics
	ADVANCED DIGITAL DESIGN WITH VHDL
	Date: Saturday, 18-11-2017 Max. Marks: 70 02.30 PM to 05.00 PM Max. Marks: 70
Instru	 ctions: 1) Attempt five questins. 2) Q. (1) and (2) are compulsory. 2) Answer any three questions from Q.3 to Q.7. 3) Figures to the right indicates full marks.
Q.1	A) Choose the alternatives given below. 08 1) The are the programming technologies used for PLD. 08 a) SRAM b) EPROM c) Flash d) All of these
	 2) The FPGA architecture are based on to generate logic functions. a) LUT b) Multiplexer c) Macrocell d) Both a & b
	 3) The VHDL supports design methodology. a) Top – down b) Bottom – up c) Mixed d) All of these
	 4) The Generate statement is statement. a) Sequential b) Concurrent c) Process d) All of these
	5) The adding operator used in VHDL. a) '+' b) '-' c) '&' d) All of these
	 6) The meaning of 'H' is in Data types STD_LOGIC_1164. a) High b) 1 c) Weak 1 d) All of these
	 7) The GENERIC statement is declared in of the VHDL code. a) Architecture b) Entity c) Process d) All of these
	 8) The mode of ports in entity declaration are types. a) 2 b) 3 c) 4 d) None of these4
	 B) State True of False. 1) The wait statement provides an alternate way to suspend the execution of a process.
	 The place and route tool belongs to front end design process. The component declaration is appeared in the declaration part of architecture.
	The LOOP statement is used to iterate through the set of concurrent

4) The LOOP statement is used to iterate through the set of concurrent statement.

Set P

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	5)	The generic and constant values are assigned by ':=' assignment operator.	
	6)	The process statement is itself a concurrent statement.	
Q.2	a) b)	Attempt any two. (Short questions) State in brief features of VHDL. Explain the CPLD. Write a note on Macrocell.	10
	B)	Explain the entity using controlled inverter.	04
Q.3	-	Discuss the basic language element of VHDL? Explain identifier and operators in detail.	05
	•	Write the VHDL code for 8 to 1 multiplexer.	05
Q.4		Explain the various types of architecture bodies for VHDL with suitable example.	09
	b)	Write VHDL code for decade counter.	05
Q.5	a)	Explain the PLD design flow for IC fabrication. Example the EDA tools for PLD.	09
	b)	Write VHDL code for 8 to 3 encoder.	05
Q.6		Give the detail classification of PLD devices. Explain the FPGA in detail. Write VHDL code for 4 – bit gray to binary code.	09 05
Q.7		Explain the Attributes and Generic for VHDL. Write VHDL code for ALU using concurrent statement.	09 05

Electronics **Instructions:** 1) Attempt five questions. 2) Q. (1) and (2) are compulsory. 2) Answer any three questions from Q.3 to Q.7. 3) Figures to the right indicates full marks. A) Choose the alternatives given below. 1) _____ type of non-previleged processor mode is entered due to raising of high priority of an interrupt. a) User mode b) Fast interrupt mode (FIQ) c) Interrupt mode (IRQ) d) Supervisor mode (SVC)

2) ____ instructions are called Program Status Register transfer instructions.

a) LDR, STR	b) LDM, STM
c) MCR, MRC	d) MSR, MRS

- 3) What are the values of the I and F bits in the Program Status Register on reset?
 - a) I=0, F=0 b) I=1, F=1 c) I=0. F=1 d) I=1. F=0
- 4) The glue logic that connects the memory system to the AMBA bus logic and control.
 - a) Main memory b) Reset
 - c) ARM core d) Glue logic
- 5) In LPC 2148, when internal reset is removed the processor begins executing at _____.
 - a) Address 0 b) Address 1
 - c) Address 5 d) Address 7
- 6) ______ vector is called when you execute a SWI instruction.
 - a) Undefined instruction b) Reset c) Software interrupt
 - d) Perfetch abort
- 7) The memory map address ______ is reserved for the vector table.
 - a) 0xFFFFFFF b) 0x000000AA d) 0x0000000
 - c) 0x00000FF
- 8) _____ register is accessible in all processor modes. b) Bank register

a) Link register

- c) Unbanked register
- d) Current program register

B) State True or false.

- 1) The ARM core uses the Link register to monitor and control internal operations.
- 2) All instructions in ARM are conditionally executed.

M.Sc.	(Semest	er - III)

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Q.1

Day & Date: Tuesday, 21-11-2017 Time: 02.30 PM to 05.00 PM

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Max. Marks: 70

		 Swap is a load- store instruction. The ARM processors does not support to the byte address. The CPSR has two interrupt mask bits, 7 and 6 to control the masking of IRQ and FIQ, respectively. User mode is non – privileged mode. 	
Q.2	A)	 Attempt any two. 1) State and explain the nomenclature used ARM processor with example. 2) Compare ARM, Jazzal and Thumb instruction set. 3) Discuss the features of ARM LPC 2148. 	10
	B)	Explain the clock and reset circuit of ARM LPC 2148.	04
Q.3	a)	Describe the design of ARM microcontroller based system for temperature measurement.	08
	b)	Write a note on I/O ports of ARM LPC 2148.	06
Q.4		Explain ARM bus architecture in brief. Explain watch dog timer.	08 04
Q.5	Ĩ	 Give the functions of following registers in ARM processor. i. Stack Pointer ii. Link register iii. Program counter Write a note on barrel shifting. 	08 06
Q.6	a)	Write embedded c program to interface LED to ARM microprocessor with suitable diagram. Write a note on I/O ports of ARM LPC 2148.	08 06
Q.7	a)	Explain on-chip UART of ARM microcontroller. Draw the block diagram of ARM LPC 2148.	08 06

06

Day & Date: Tuesday, 21-11-2017 Time: 02.30 PM to 05.00 PM	Max. Marks: 70
 Instructions: 1) Attempt five questions. 2) Q. (1) and (2) are compulsory. 2) Answer any three questions from 3) Figures to the right indicates for any figures to the right indicates for any figures for any figures for any figures for the right indicates for any figures for any figu	om Q.3 to Q.7.
 Q.1 A) Choose the alternatives given below 1) Guard ring are used to a) Prevent latchup b) Collect injected majority carries c) Collect injected minority carries d) All of these 	rs
2) For pseudo-nMOS inverter the gaa) VDDc) Output	te of the p-device is connected to b) Ground d) Floating
 3) In Silicon on Insulator (SOI) a) Sapphire c) Silicon 	is used as substrate. b) Magnesium aluminate spinel d) Both a & b
 4) In VLSI design, aggregates are constance c) Tools 	bmmonly referred to as b) Cells d) Both a & b
5) Fall time is the time for a waveform value.a) 50% to 10%c) 90% to 10%	m to fall from of its steady state b) 90% to 50% d) 50% to 20%
6) The basic raw material used in CNa) Disk of siliconc) Both a & b	b) Water of silicon
 7) Absolute value of threshold voltag temperature. a) Decrease c) Constant 	je decreases with an in b) Increase d) None of these
 8) In CMOS capacitor the dielectric r a) 100 nm SiO₂ c) 10 nm SiO₂ 	material used is b) 10 μ m SiO ₂ d) 100 μ m SiO ₂

B) State True or false.

- 1) Photoresist material is used as mask in fabrication process
- 2) An increase in the temperature of an MOS device result in decrease in carrier mobility.
- 3) Voltage transfer characteristics of CMOS inverter are independent of ratio β_n/β_p .

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M.Sc. (Semester - III) (New) (CBCS) Examination Oct/Nov-2017 **Electronics CMOS DESIGN TECHNOLOGIES**

Seat No.

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		4) Static power dissipation occurs due to charging and discharging of load	
		 capacitance. 5) For DC characteristics of CMOS inverter in D region n devices is in non-saturated region and p device is in saturated region. 6) In PMS design environment P stands for process. 	
Q.2		 Attempt any two. 1) Explain Noise margin. 2) Write a note on circuit elements in CMOS process. 3) Explain power dissipation. Derive an expression for threshold voltage. 	10 04
Q.3		What do you mean by stick diagram? Draw a stick diagram for two input multiplexer. Describe the steps involved in silicon semiconductor technology.	08 06
Q.4		Explain the n-well process for fabrication of MOS device. Explain pseudo n-MOS inverter.	08 06
Q.5		Explain the DC characteristics of CMOS inverter. Write a note on Hierarchy.	08 06
Q.6		Describe the switching characteristics of CMOS. Write a note on Y - diagram.	08 06
Q.7	-	Explain the nMOS enhancement transistor in detail. Write a note on Views.	08 06

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Seat No.		Set	Ρ
	M.Sc. (Semester - II	I) (Old) (CBCS) Examination Oct/Nov-2017 Electronics	
	Advanced [Digital Systems Design with VHDL	
	Date: Saturday, 18-11-20 2.30 PM to 05.00 PM		s: 70
Instruc	,		
	 A) Choose the alternati 1) The VHDL supports _ a) Top-down c) Mixed 	ves given below. design methodology. b) Bottom-up d) All of these	08
2	2) The meaning of '1' is a) High c) Forcing 1	in Data Types STD_LOGIC_1164. b) 1 d) All of these	
:	 The design a) Design entry c) Both a & b 	n process is included in front end design. b) Gate level netlist d) None of these	
	4) The NAND and NORa) Distributivec) Cumulative	operators are not b) Associative d) None of these	
:	5) The component declaa) Namec) Both a & b	ration declares the of the component. b) Interface d) None of these	
	6) The mode of ports ina) 2c) 4	entity declaration are types. b) 3 d) None of these	
	7) The value a) Variable c) Constant	is assigned by <= assignment operator. b) Signal d) All of these	
	8) The FPGA architectura) LUTc) Macrocell	re are based on to generate logic functions. b) Multiplexer d) Bothe a & b	
	B) State True of False. 1) Simulation is a logica	I way of emulating the behavior of a circuit.	06
:	2) In architecture for an	entity, all statements are concurrent.	
	3) The place and route t	ool belongs to back end design process.	
	4) The process stateme	nt is itself a concurrent statement.	
:	 The wait statement process. 	rovides an alternate way to suspend the execution of a	
	6) The component decla	ration is appeared in the declaration part of entity.	

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Q.2	 A) Attempt any two. (Short questions) a) Explain the entity using decoder. b) Discuss capabilities and features of VHDL. c) Discuss EDA tools for PLD design flow. 	10
	B) Explain the SPLD.	04
Q.3	a) State and explain the different types of architecture bodies for full adder.b) Write the VHDL code for 4 – bit shift register.	09 05
Q.4	 a) Explain the process statement with the syntax. Explain any three statements. b) Write VHDL code for ALL using consurrent code 	09
	b) Write VHDL code for ALU using concurrent code.	05
Q.5	a) What do you mean by basic language element? Explain identifier and Data objects in detail.b) Write VHDL code for 8:1 Demultiplexer.	09 05
	b) while verbe code for 6.1 Demuniplexer.	05
Q.6	 a) Explain in detail classification PLD devices. Explain the architecture of FPGA. 	09
	b) Write VHDL code for 4 – bit binary to gray code.	05
Q.7	a) Explain the packages and libraries for VHDL.b) Write VHDL code for decade counter.	09 05